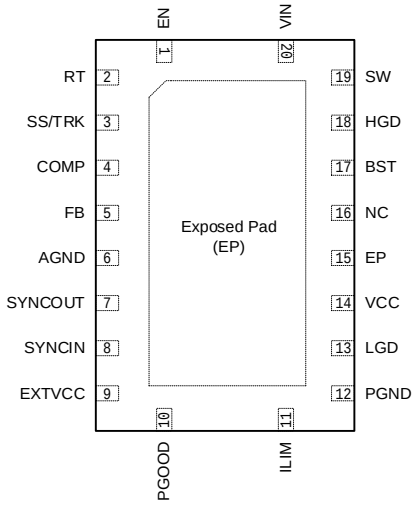
Revision 1.0: Released to Market
Revision 1.1: Update FEATURES information
Revision 1.2: Update Package information
Revision 1.3: Delete error description

SCT82A34DHKR	Tape & Reel	3000	2A34	20	DFN3.5X4.5-20L

Over operating free-air temperature unless otherwise noted(1)

VIN	-0.3	105	V
SW	-1	105	V
SW (20ns transient)	-5	105	V
ILIM	-1	105	V
EN	-0.3	105	V
VCC, EXTVCC,LO	-0.3	14	V
FB, COMP, SS/TRK, RT	-0.3	5	V
SYNCIN	-0.3	14	V
BST	-0.3	115	V
BST to VCC		105	V
HO,BST to SW	-0.3	14	V



Top View: DFN3.5X4.5-20L

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EN	1	I	Enable input and under voltage lockout programming pin. If the EN voltage is below 0.41V, the controller is in the shutdown mode with all functions disabled. If the EN voltage is greater than 0.41V and less than 1.2 V, the regulator is in standby mode with the VCC regulator operating, the SS pin grounded, and no switching at the HGD and LGD outputs. If the EN voltage is above 1.2V, the SS/TRK voltage can ramp and pulse-width modulated gate-drive signals are delivered to the HGD and LGD pins. The user can use EN pin program input under voltage lockout UVLO threshold. A 10μA current source is enabled when EN exceeds 1.2 ų ulm e e

SYNCIN	8	I

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$R_{\theta JA}$ $R_{\theta JC\ (top)}$	Junction to ambient thermal resistance(1)	37	°C/W

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	5.5	100	V
VCC	External VCC bias rail	8	13	V
EXTVCC	External EXTVCC bias rail	4.7	13	V
T_J	Operating junction temperature	-40	125	°C

V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014			

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V_{COMP_L}	COMP output low voltage	COMP sinking 1mA		0.25		V

V_{EN_SHDN}	Shutdown to standby EN threshold	V_{EN} rising		0.41	0.48	V
	Hysteresis			30		mV
V_{EN}	Standby to operating EN threshold	V_{EN} rising	1.02	1.2	1.44	V
I_{EN_HYS}	Standby to operating hysteresis	V_{EN}=1.5V	9	10	11	μA

I_{SS}	SS/TRK capacitor charging current	$V_{SS/TRK}$=0V	8.5	10	12	uA
R_{SS}	SS/TRK discharging FET resistance	V_{EN}=1V, $V_{SS/TRK}$=0.1V		12		Ω
V_{SS-FB}	SS/TRK to FB offset			62		mV
V_{CC_CLAMP}	SS/TRK clamp voltage	$V_{SS/TRK}$ – V_{FB}, V_{FB}=0.8V		120		mV

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$D_{100K(MAX)}$	Maximum duty cycle	F_{SW}=100kHz, 5V<V_{IN}<100V	98	%
$D_{400K(MAX)}$	Maximum duty cycle	F_{SW}=400kHz, 5V<V_{IN}<100V	92	%
$V_{RAMP(MIN)}$	Ramp valley voltage (COMP at 0% duty cycle)		300	

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Figure 1. Efficiency vs Load Current, Vout=12V, DCM

Figure 2. Efficiency vs Load Current, Vout=12V, FCCM

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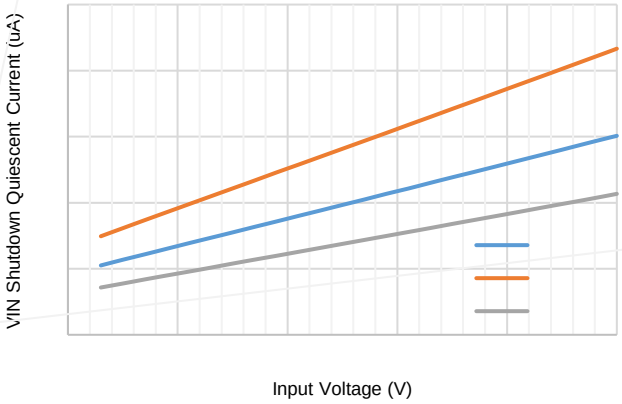

Figure 7. $I_{SHUTDOWN}$ vs Input Voltage

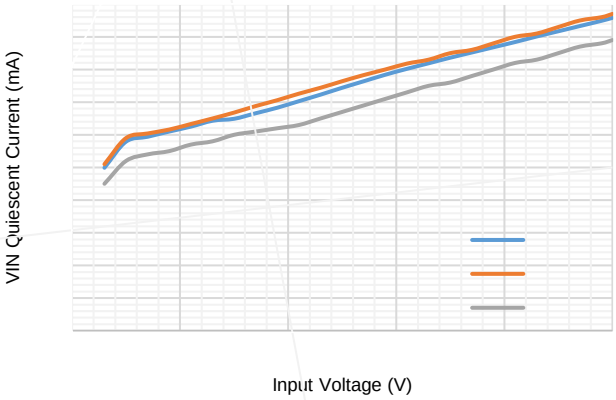

Figure 8. I_Q vs Input Voltage

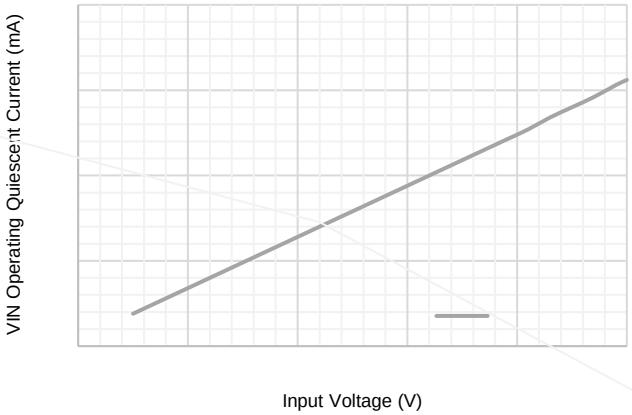

Figure 9. VIN Quiescent Current with External VCC Applied

Figure 10. ILIM Current Source vs TJ

Figure 11. SS/TRK Current Source vs TJ

Figure 12. Gate Driver Peak Current vs VCC Voltage

Figure 13. HO Driver Resistance vs VCC Voltage

Figure 14. LO Driver Resistance vs VCC Voltage

Figure 15. $t_{ON(MIN)}$ and $t_{OFF(MIN)}$ vs TJ

Figure 16. Deadtime vs TJ

Figure 17. VCC Voltage vs InpĞ

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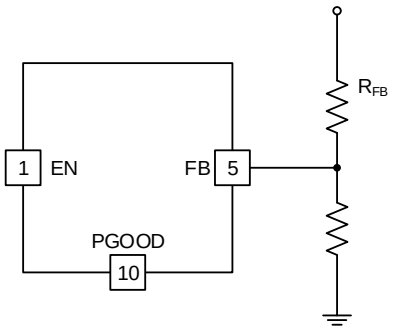

Figure 23. Master-Slave Sequencing Power up Using PGOOD and EN

To adjust frequency for optimizing external components for various applications, the system designer can connect a resistor from the RT pin to AGND or synchronize the SCT82A34 to an external clock signal through the SYNCIN pin.

A free-running switching frequency can be programmed from 100KHz to 1.2MHz by using a resistor from the RT pin to AGND. The frequency set resistance R_{RT} is calculated by Equation 5. Standard-value resistors for common switching frequencies are given in Table 1.

[redacted] (5)

Table 1. Frequency Set Resistor R_T

100	100
2 Ŷ صلعم e ǰ ξ	

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2Ŷ 100 t T 100

The

Two optional connections sensing inductor current:

$R_{DS(on)}$ sensing mode: R_{ILIM} is tied to SW to use the RDS(on) of the low-side MOSFET as a sensing element.

R_{SENSE} shut mode: R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET.

The SCT82A34 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly. The ILIM current with RDS-ON sensing is 200 μA at 27°C junction temperature and incorporates a TC of +4500 ppm/℃ to generally track the RDS(on) temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100μA in RSENSE mode. This controls the valley of the inductor current during a steady state.

Depending on the chosen mode, select the resistance of RILIM using Equation 6 or Equation 7.

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The SCT82A34 integrates the voltage mode control loop implementation and feeds the input voltage forward to eliminate the input voltage dependence of the PWM modulator gain. The voltage mode buck control loop is show as below:

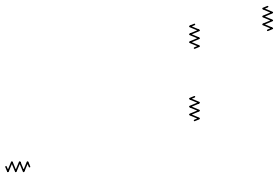

Figure 25. Buck circuit voltage loop control diagram

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, RFB2 , has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature.

The small-signal open-loop response of a buck regulator is the product of modulator, power train and compensator transfer functions. The power stage transfer function can be represented as a complex pole pair associated with the output LC filter and a zero related to the ESR of the output capacitor. The DC (and low frequency) gain of the modulator and power stage is V_{IN} /V_{RAMP} . The gain from COMP to the average voltage at the input of the LC filter is held essentially constant by the PWM line feedforward feature of the SCT82A34 (KFF=V_{IN} /V_{RAMP} =15 V/V).

Complete expressions for small-signal frequency analysis are presented in Table 2. The transfer functions are denoted in normalized form. While the loop gain is of primary importance, a regulator is not specified directly by its loop gain but by its performance related characteristics, namely closed-

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Table 3. Buck Regulator Poles and Zeros

POWER STAGE POLES	POWER STAGE ZEROS	COMPENSATOR POLES	COMPENSATOR ZEROS
$_{o}$ $\frac{1}{\sqrt{L \ C_{OUT}}}$	$_{ESR}$ $\frac{1}{R_{ESR} \ C_{OUT}}$	$_{p1}$ $\frac{1}{R_{C1} \ C_{C2}}$	$_{z1}$ $\frac{1}{R_{C1} \ C_{C1}}$
		$_{p2}$ $\frac{1}{R_{C2} \ C_{C3}}$	$_{z2}$ $\frac{1}{R_{FB1} \ R_{C2}) \ C_{C3}}$

Figure 27 shows the open-loop response gain and phase. The poles and zeros of the system are marked with x and o symbols, respectively, and a + symbol indicates the crossover frequency. When plotted on a log (dB) scale, the open-loop gain is effectively the sum of the individual gain components from the modulator, power stage, and compensator. The open-loop response of the system is measured experimentally by breaking the loop, injecting a variable-frequency oscillator signal, and recording the ensuing frequency response

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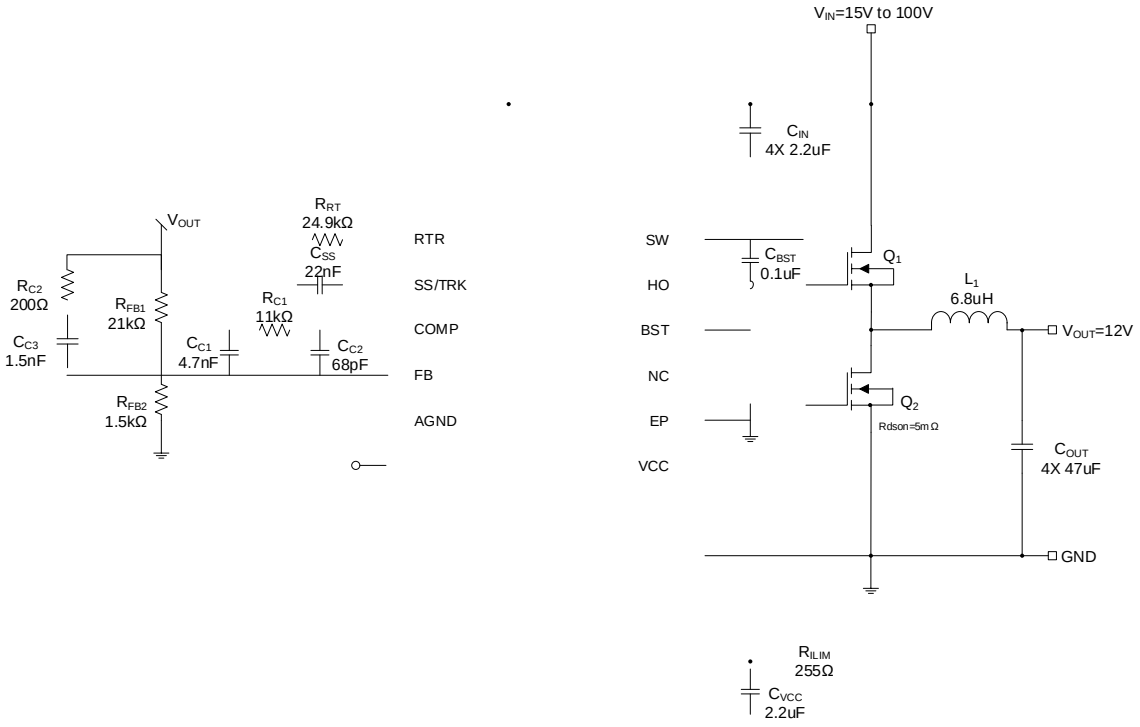

Figure 28. Application Schematic, 48V to 12V, 8A Buck Regulator at 400kHz

Input Voltage	48V Normal 15V to 100V
Output Voltage	12V
Maximum Output Current	8A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	50mV
Transient Response 1.25A to 3.75A load step	ΔVout = 200mV
Start Input Voltage (rising VIN)	13.8V
Stop Input Voltage (falling VIN)	12.4V

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Vin=48V, Vout=12V, unless otherwise noted

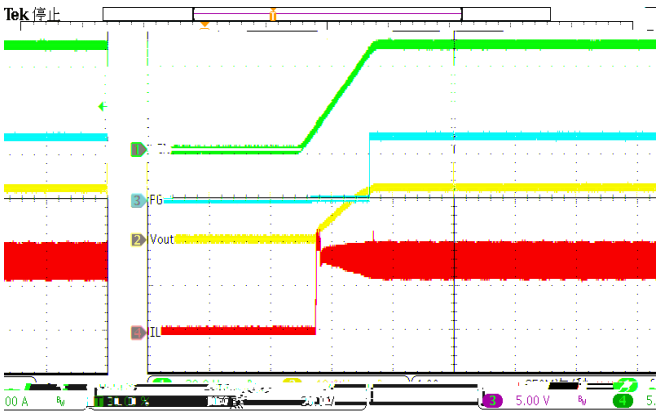

Figure 29. Power up(Iload=8A)

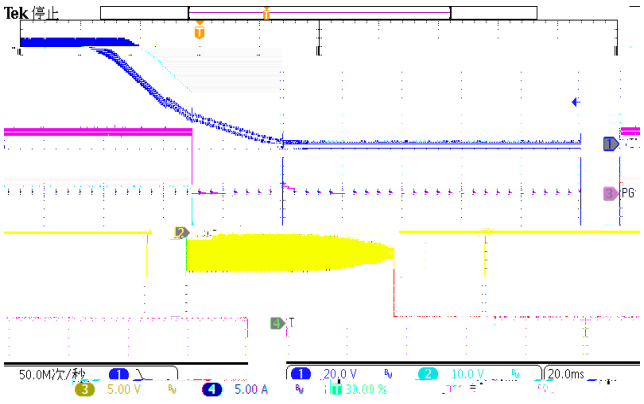

Figure 30. Power down(Iload=8A)

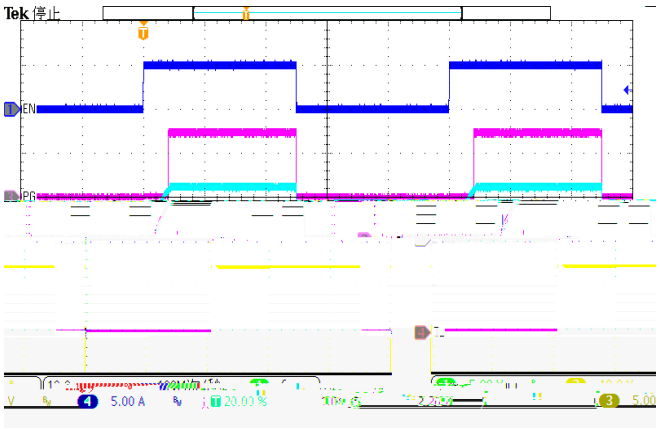

Figure 31. Enable (Iload=8A)

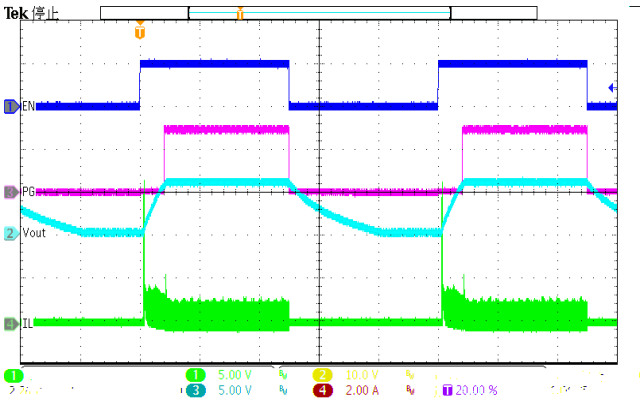

Figure 32. Enable (Iload=0.1A)

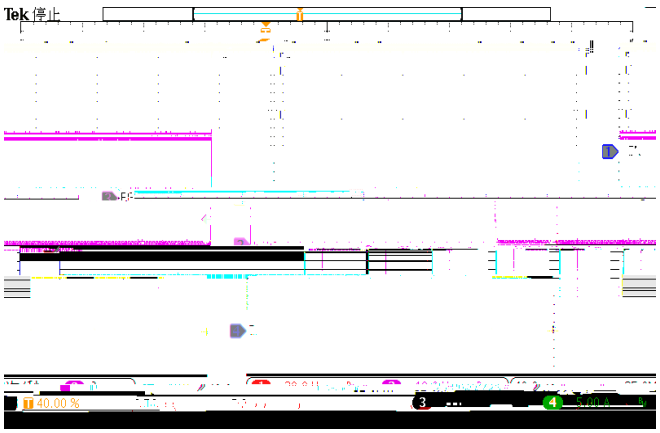

Figure 33. Normal to Hard Short

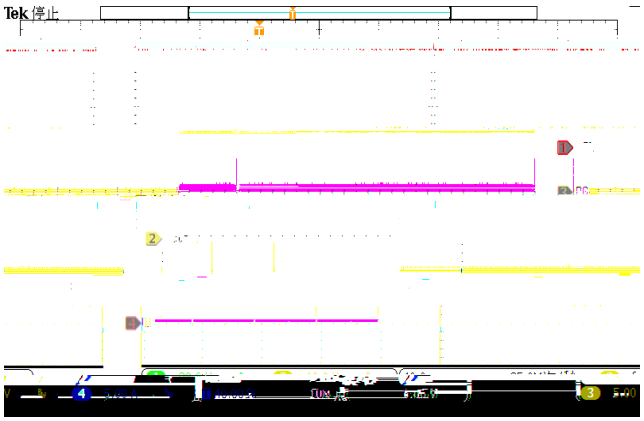

Figure 34. Hard Short Recovery

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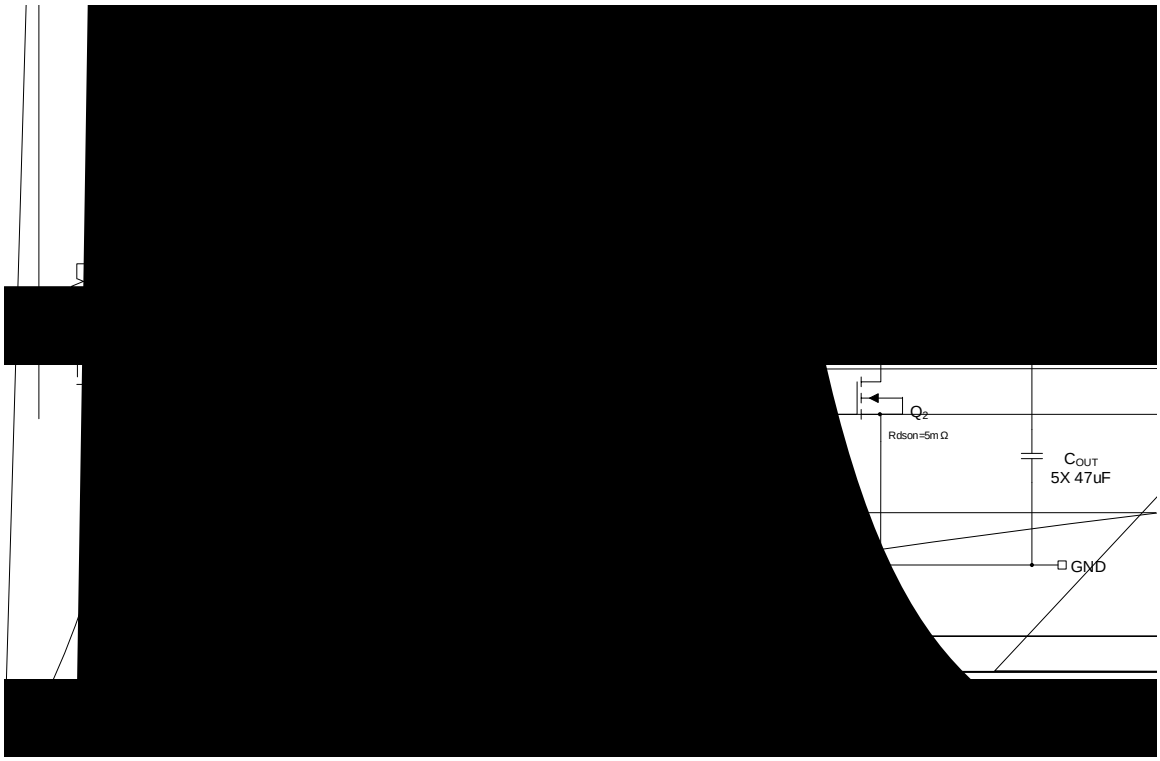

Input Voltage	48V Normal 7V to 100V
Output Voltage	5V
Maximum Output Current	20A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	16mV
Transient Response 5A to 15A load step	ΔVout = 420mV
Start Input Voltage (rising VIN)	6.3V
Stop Input Voltage (falling VIN)	5.1V

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Vin=48V, Vout=5V, unless otherwise noted

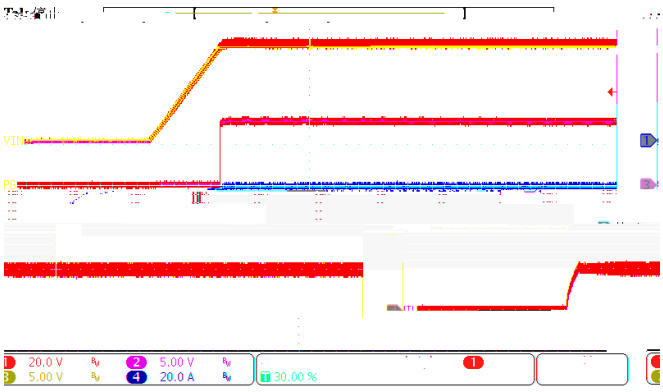

Figure 42. Power up(Iload=20A)

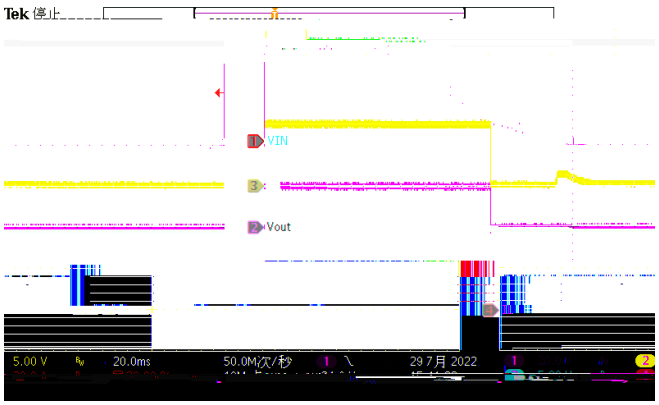

Figure 43. Power down(Iload=20A)

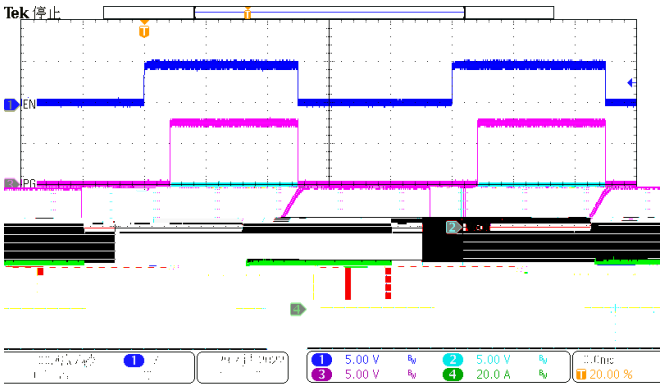

Figure 44.Enable (Iload=20A)

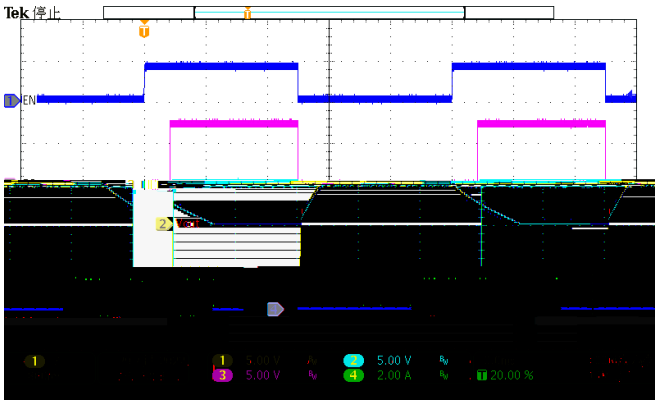

Figure 45. Enable (Iload=0.1A)

Figure 46. Normal to Hard Short

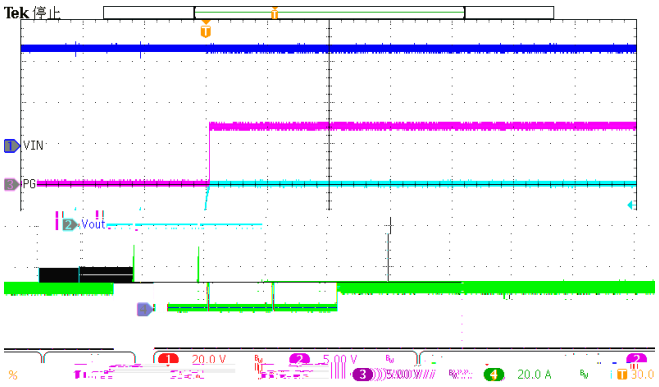

Figure 47. Hard Short Recovery

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For PCB power loop design, as shown in Figure. 54, the distance between Q1 and Q2 shall be minimized, and the input capacitance 100nF shall be as close as possible to the drain of Q1 and the power ground. The inductance shall be close to the switching node to minimize the current loop. The small area of the buck regulator hot loop is denoted by the white arrow in Figure 54. This is critical to minimize EMI as well as switch-node voltage overshoot and ringing.

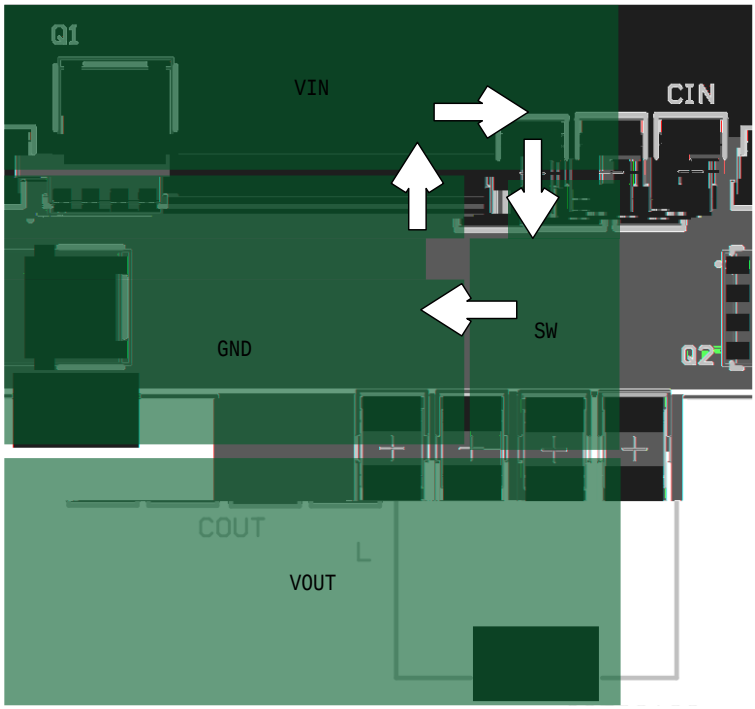

Figure 54. Power stage PCB Layout

Figure 55 shows an example PCB layout based on the SCT82A34 design. In order to prevent the PGND from interfering with the controller AGND, It is recommended to use a single point connection between the two ground.

Figure 55. Controller PCB Layout

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